

TENTATIVE

CM200DC1-24NFM

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Apr.	Y.Nagashima 28-July-'08			Y.Nagashima 27-Oct-'08

HIGH POWER SWITCHING USE

Notice: This is not a final specification. Some parametric limits are subject to change.

CM200DC1-24NFM

I_c 200A
 V_{CES} 1200V
 Flatbase Type / Insulated Type / Copper base type
 2-elements in a pack
 RoHS Directive compliant

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Caution: No short circuit capability is designed.

APPLICATION
 Welder only.

ABSOLUTE MAXIMUM RATINGS ($T_j=25^\circ\text{C}$, unless otherwise specified)

Symbol	Item	Conditions	Ratings	Units
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	± 20	V
I_c	Collector current	Operation	200	A
I_{CM}		Pulse ^{*4}	300	
I_E ^{*3}	Emitter current	Operation	150	A
I_{EM} ^{*3}		Pulse ^{*4}	300	
P_c ^{*5}	Maximum collector dissipation	$T_c=25^\circ\text{C}$ ^{*1}	1340	W
T_j	Junction temperature		- 40 ~ +150	$^\circ\text{C}$
T_{stg}	Storage temperature		- 40 ~ +125	$^\circ\text{C}$
V_{iso}	Isolation voltage	Main terminal to base plate, AC 1 min.	2500	V
-	Torque strength	Main terminal M6	3.5 ~ 4.5	N·m
-	Torque strength	Mounting holes M6	3.5 ~ 4.5	N·m
-	Weight	Typical value	310	g

ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

Symbol	Item	Conditions	Min.	Typ.	Max.	Units	
I _{CEs}	Collector cutoff current	V _{CE} =V _{CEs} , V _{GE} =0V	-	-	1	mA	
V _{GE(th)}	Gate-emitter threshold voltage	I _c =20mA, V _{CE} =10V	4.5	6.0	7.5	V	
I _{GES}	Gate leakage current	±V _{GE} =V _{GES} , V _{CE} =0V	-	-	0.5	μA	
V _{CE(sat)}	Collector to emitter saturation voltage	I _c =200A ^{*6} V _{GE} =15V	T _J =25°C	-	2.9	3.8	V
			T _J =125°C	-	2.9	-	
C _{ies}	Input capacitance	V _{GE} =0V, V _{CE} =10V ^{*6}	-	-	35	nF	
C _{oes}	Output capacitance		-	-	3.0		
C _{res}	Reverse transfer capacitance		-	-	0.68		
Q _G	Total gate charge	V _{CC} =600V, I _c =200A, V _{GE} =15V	-	1000	-	nC	
t _{d(on)}	Turn-on delay time	V _{CC} =600V, I _c =200A	-	-	300	ns	
t _r	Turn-on rise time	V _{GE1} =V _{GE2} =15V, R _G =1.6Ω	-	-	80		
t _{d(off)}	Turn-off delay time	Inductive load	-	-	500		
t _f	Turn-off fall time	switching operation	-	60	200		
t _{rr} ^{*3}	Reverse recovery time	I _E =150A	-	70	150		
Q _{rr} ^{*3}	Reverse recovery charge		-	6	-	μC	
V _{EC} ^{*3}	Emitter-collector voltage	I _E =150A, V _{GE} =0V	-	2.8	3.5	V	
R _{th(j-c)Q}	Thermal resistance	IGBT part (1/2 module) ^{*1}	-	-	0.093	°C/W	
R _{th(j-c)R}		FWDi part (1/2 module) ^{*1}	-	-	0.23		
R _{th(c-f)}	Contact thermal resistance	Case to fin, Thermal grease applied (1/2 module) ^{*1 *2}	-	0.02	-		
R _G	External gate resistance		1.6	-	16	Ω	

*1: T_c, T_r measured point is just under the chips. (Refer to the figure of the chip location.)

*2: Typical value is measured by using grease of λ=0.9W/(m·K). [ex Shin-Etsu Chemical Co.,Ltd / Silicone Fluid Compound "G-747"]

*3: I_E, I_{EM}, V_{EC}, t_{rr} & Q_{rr} represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).

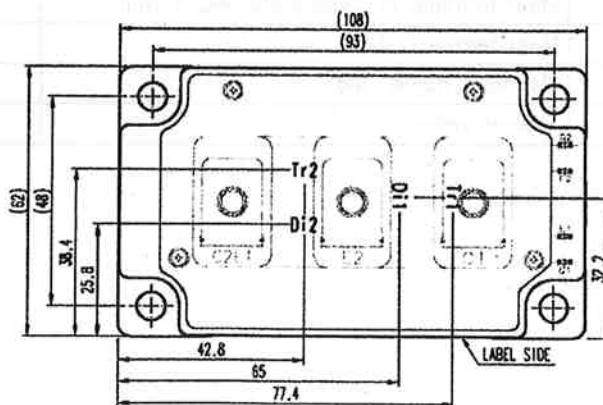
*4: Pulse width and repetition rate should be such that the device junction temperature (T_J) dose not exceed T_{Jmax} rating.

*5: Junction temperature (T_J) should not increase beyond 150°C.

*6: Pulse width and repetition rate should be such as to cause negligible temperature rise. (Refer to the Fig.4 and Fig.5)

Fig.1 Chip Location (Top view)

Dimensions in mm



Each mark points the center position of each chip. Tr1&Tr2 : IGBT , Di1&Di2 : FWDi.

Fig2 OUTLINE DRAWING

Dimensions in mm

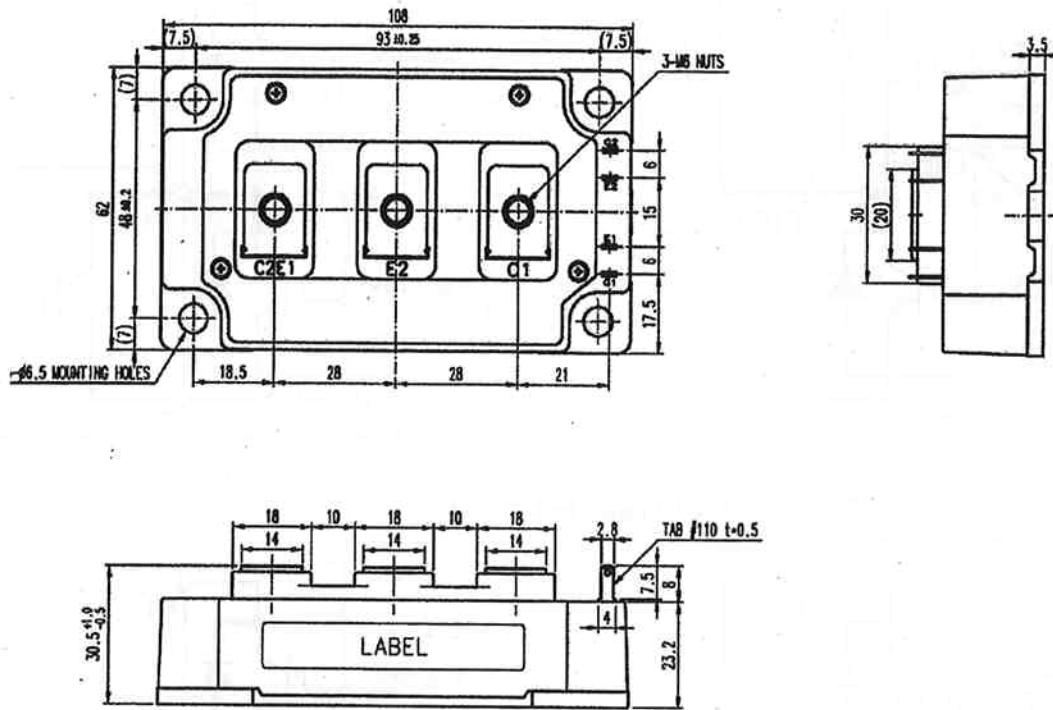
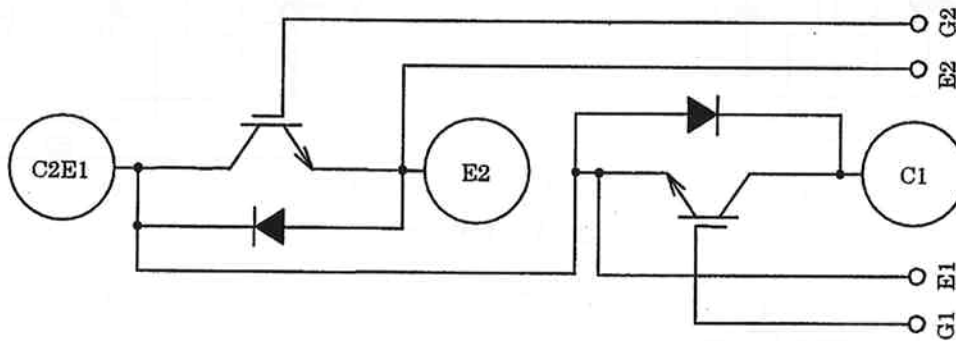


Fig.3 CIRCUIT DIAGRAM



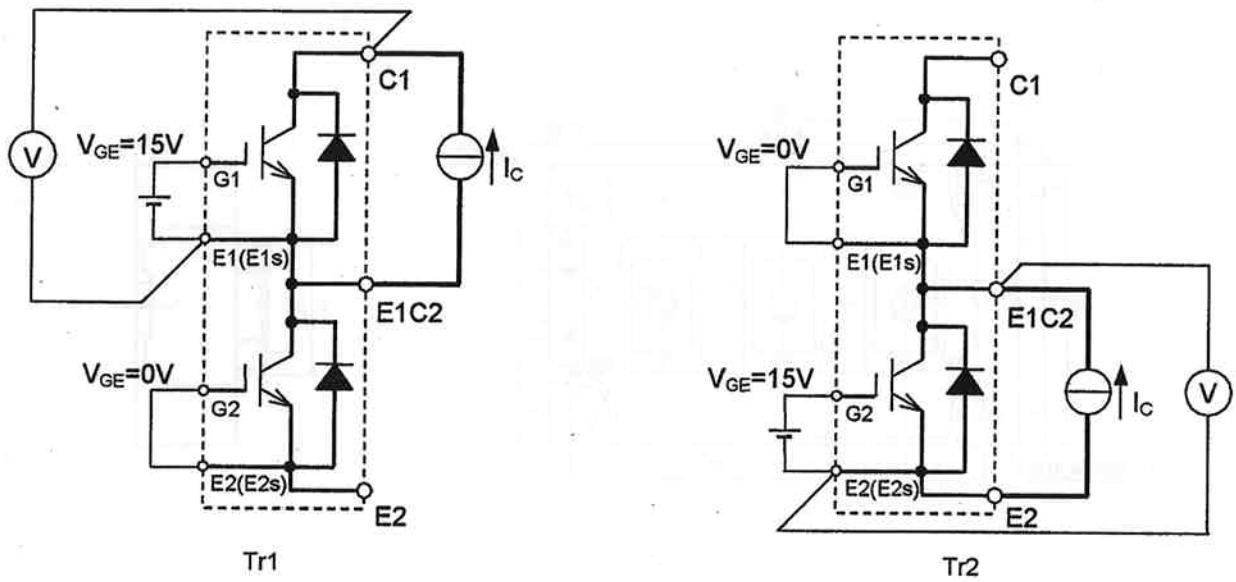


Fig.4 $V_{CE(sat)}$ test circuit

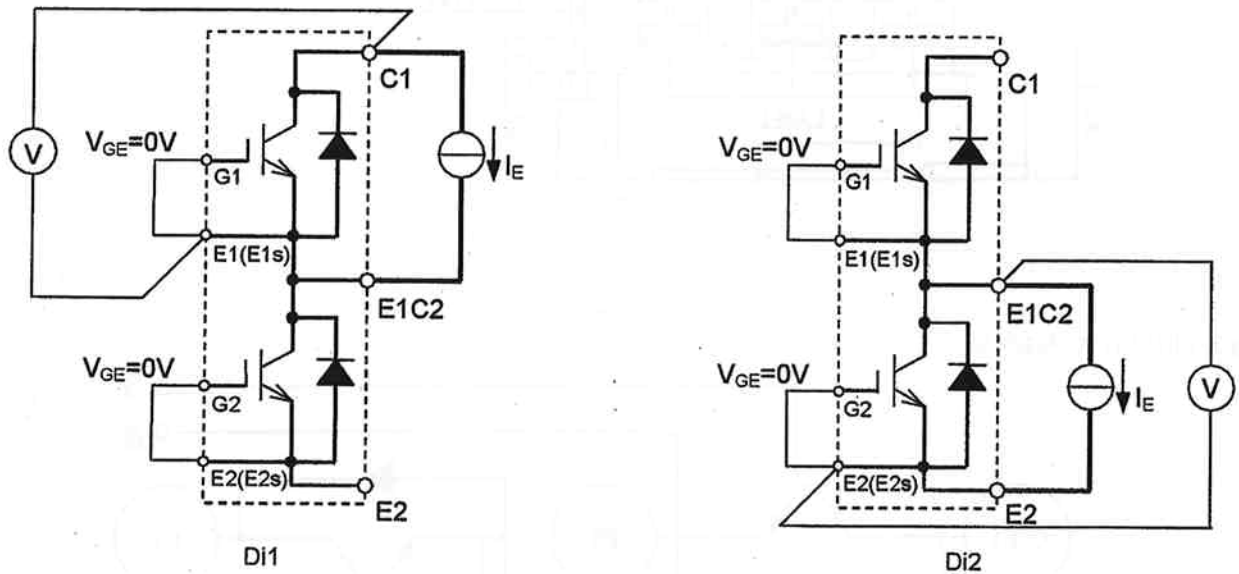


Fig.5 V_{EC} test circuit

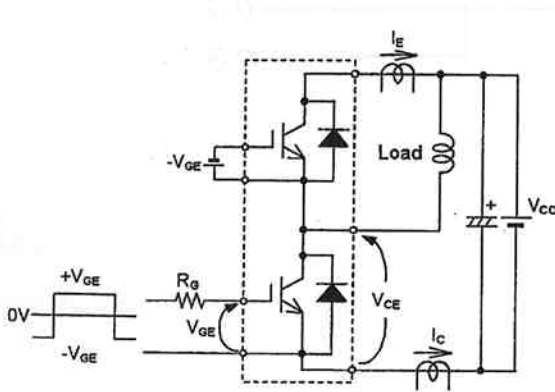


Fig.6 Switching time test circuit and waveforms

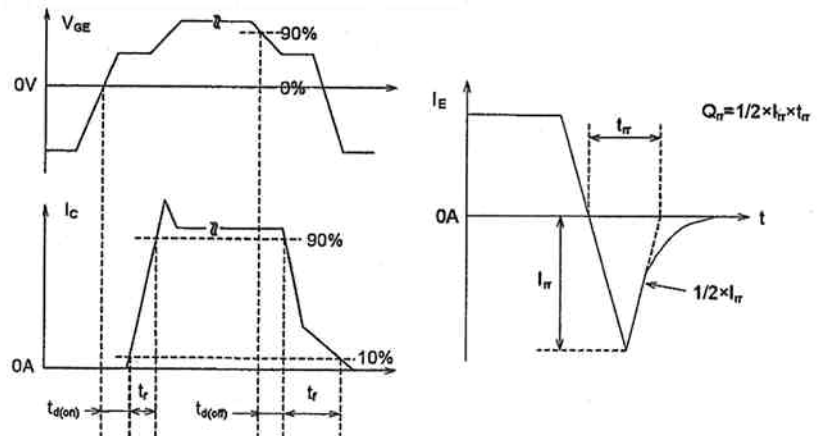


Fig.7 t_{rr} , Q_{rr} test waveform

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